Change Summary

CHANGES

No.	Applicable Section(s)	Description	Page(s)

REVISION HISTORY

Revision No.	Revision Summary	Release Date
0.5	Initial release	11/02/2012

LED Driver Controller with Primary Side Control and Power Factor Correction

FEATURES

- Primary side control AC/DC converter controller
- High Power Factor with wide range input voltage
- Constant Current Output
- 3-level analog dimming control using a wall switch
- Fixed operating frequency
- Built-in high-voltage startup circuit
- Compatible with neon indicators in wall switch
- Provides protection functions
  - VDD Over voltage protection
  - VDD Under voltage lockout with hysteresis
  - Open LED protection
  - Short LED protection
  - Primary-side cycle by cycle current limit
  - Maximum gate drive output clamp
  - Over-temperature protection

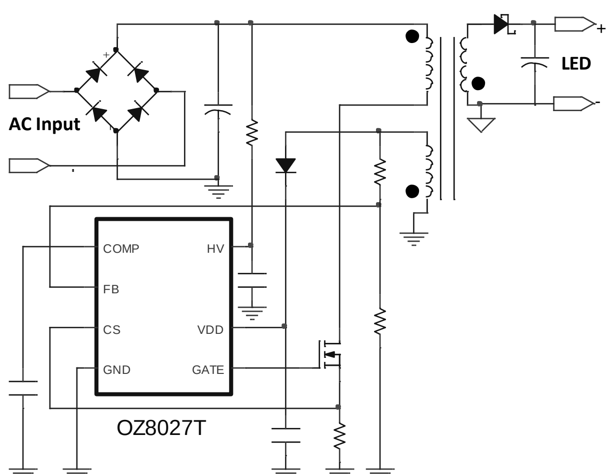
APPLICATIONS

- LED lighting

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ8027TGN	-20ºC to +85ºC Note(3), page 3	SOP-8 Lead-Free

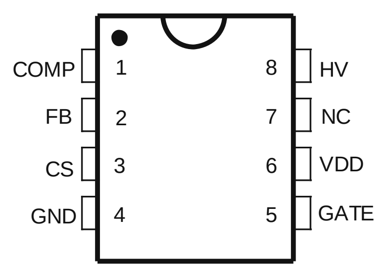
SIMPLIFIED OPERATING CIRCUIT



GENERAL DESCRIPTION

OZ8027T is a primary-side control LED driver controller. The controller can be used in high power factor AC/DC converter applications. It provides a proprietary technology of controlling LED brightness by the ON/OFF of an AC wall switch. The controller operates at a fixed frequency of 67 kHz with discontinuous current mode (DCM) in Flyback circuit topology. Built in with a high-voltage start-up circuit, OZ8027T eliminates start-up resistors in applications. It works with neon indicators in a traditional wall switch without interference. OZ8027T provides protection features including VDD under-voltage lockout and over voltage protection, cycle by cycle current limit and over current protection at current sense circuit, open LED protection, short LED protection, over temperature protection. The driver output voltage is clamped to protect the external power MOSFET from being damaged.

PIN DIAGRAM



PIN DESCRIPTION

Name	I/O[1]	Pin No.	Description
COMP	I/O	1	Compensation; amplifier output
FB	I	2	Feedback; zero current detection
CS	I	3	Current sense
GND	GND	4	Power Ground
GATE	O	5	Gate drive output
VDD	VDD	6	Power supply input
NC	NC	7	No connection
HV	I	8	High voltage start-up

Note (1): I=Input, O=Output, I/O=Input/Output

BLOCK DIAGRAM

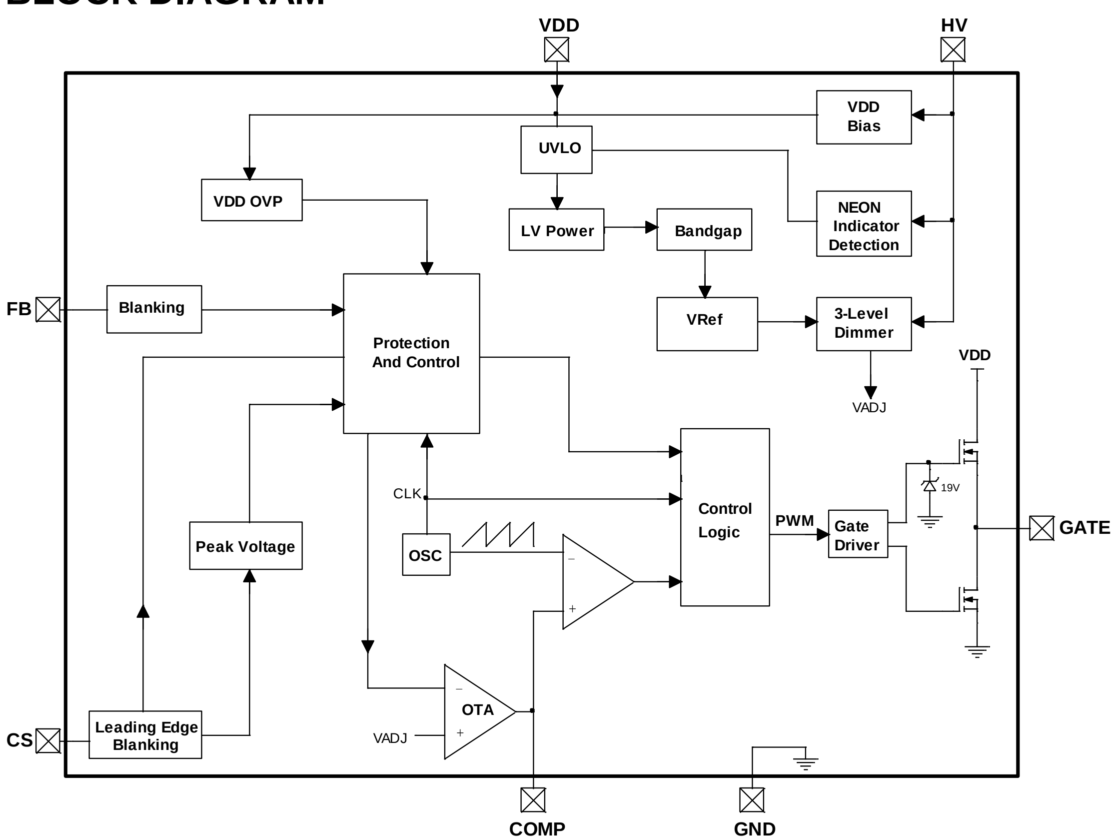


Figure 1: Block Diagram

Absolute Maximum Ratings[2]

Symbol	Parameter	Rating
V_{DD}	Maximum supply voltage to VDD pin	30.0V
V_{HV}	Input voltage to HV pin	-0.3V to 500V
V_{FB}	Input Voltage to FB Pin	-0.3V to 6.0V
V_{CS}	Input Voltage to CS Pin	-0.3V to 6.0V
V_{COMP}	Input Voltage to COMP Pin	-0.3V to 6.0V
V_{GATE}	Input Voltage to GATE Pin	-0.3V to 30.0V
ESD Capability	HBM	>2000V
	MM	>200V
T_{Max}	Maximum Operating Junction Temperature[3]	150ºC
T_{STG}	Storage Temperature Range	-55ºC to 150ºC

Note (2): The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the IC. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The "Electrical Characteristics" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

RECOMMENDED OPERATING RANGE

Symbol	Parameter	Min ~ Max
VDD	VDD Supply Voltage	11V to 24V
T_{OP-A}	Operation Ambient Temperature[3]	-20ºC to +85ºC
Thermal Impedance[3,4]	θ_{J-C}	θ_{J-A}
SOP-8	15ºC/W	110ºC/W

Note (3): Not to exceed the maximum junction temperature of the IC, which relates to the operating power of the IC and the thermal resistance of the IC/package as above. For a typical application (refer to the Reference Application Circuit, Figure 6, Page 8), the operation power of the IC can be calculated by $Pd = VDD_{IN} \times I_{IN}$, where VDD_{IN} represents the input voltage at the VDD pin of the IC and I_{IN} represents the current flow into the VDD pin of the IC.

- Using OZ8027T in an application circuit with an ambient temperature near 85^{o}C, the recommended power dissipation of the SOP-8 package is less than 400mW.
- It is recommended that the customer contact their local O2Micro Field Application Engineer (FAE), if the application is significantly different from the Reference Application Circuit in Figure 6.

Note (4): Still air, low effective thermal conductivity board per JESD51-3.

ELECTRICAL CHARACTERISTICS[5]

(T_A=25℃ and VDD=15V unless otherwise noted.)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Supply Voltage (VDD pin)						
I_{SS}	Operating Current	Gate open		1		mA
I_{DIM}	operating Current	VDD=9V		28		uA
VDD_{ON}	Turn-on Threshold Voltage			16.5		V
VDD_{OFF}	Turn-off Threshold Voltage			10.5		V
VDD_{DIM}	Reset dimming logic VDD voltage			5		V
VDD_{OVP}	VDD Over Voltage Protection			27		V
HV pin						
I_{HV}	Charge VDD current from HV pin	HV=50V, VDD=0V		1.48		mA
I_{HV_LEAK}	Leakage Current after Start-up	HV=500V, VDD>VDD_{ON}			60	uA
Internal OTA (COMP pin)						
V_{ADJ}	Reference voltage for OTA input (VADJ)	1st Dimming		1.0		V
I_{COMP_SOURCE}	COMP maximal source current			11.3		uA
FB Pin						
V_{FBU}	Upper Clamp Voltage	1mA sink current		5.7		V
V_{FBL}	Lower Clamp Voltage	4mA source current		27		mV
V_{FB_OVP}	Over Voltage Protection Threshold at FB pin			3.6		V
V_{FB_SCP}	Short Circuit Protection Threshold at FB pin			1		V
CS Pin						
V_{CS_LIM}	Cycle by cycle Current Limit Threshold on CS pin	FB=0V		1.1		V
V_{CS_OCP}	Over Current Protection Threshold on CS pin			1.6		V
$\Delta V_{CS} / \Delta I_{FB}$	Relationship of CS voltage compensation and FB source current			20		mV/mA
T_{BLANK}	Leading-Edge Blanking Time at CS pin			400		nS
GATE Drive Output (GATE Pin)						
T_R	Rise Time	C_L=1nF		79.4		ns
T_F	Fall Time	C_L=1nF		25.1		ns
VG_{CLAMP}	Gate Clamp Voltage			17.4		V
Other						
F_{OSC1}	1st and 2nd switch Frequency			67		kHz
T_{ON_MAX}	Maximum on time			11.2		uS

Note (5): Use of this product outside the limits of the test conditions may experience in a variation of parameters from the published parameters. If additional information is needed, please consult with your O2Micro Field Application Engineer (FAE).

FUNCTIONAL DESCRIPTION

Refer to both the Block Diagram in Figure 1 and the Typical Application Circuit in Figure 6 for the following discussions. All parameters mentioned below are typical values.

High Voltage Start-up Circuit and Under Voltage Lockout

Applying the AC power (110/220V) to the rectifier will provide the initial operation of the controller. The rectified AC voltage is applied to the high-voltage pin HV through a noise filter R6 and C9. R6 should use 1206 footprint resistor. High-voltage start-up circuit shortens the start-up time while eliminating external start-up resistors. During startup, capacitor C7 is charged to 16.5V by the internal start-up circuit. The turn-on and turn-off thresholds of the controller are 16.5V and 10.5V respectively. Once the VDD reaches 16.5V, all internal circuit is in operation. Refer to Figure 2, the hysteresis is implemented to prevent abnormal turn-off due to a drop at line voltage transient conditions. When VDD drops below 10.5V, the controller shuts off the driver output while keeping the dimming function control active. The controller will be in shut-off mode with control logic being reset when VDD drops below 5.0V.

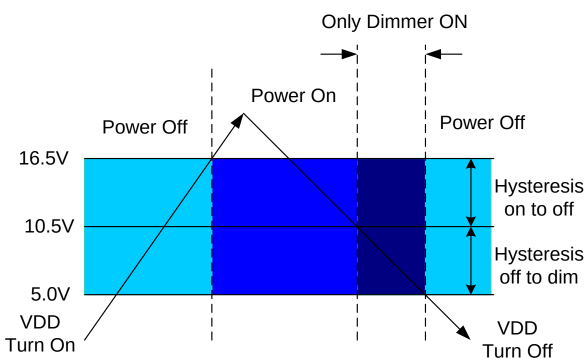


Figure 2: VDD Power Supply Hysteresis

In applications, where a neon indicator is placed in parallel with the wall switch, the neon lamp is turned on when the wall switch is set at OFF. The neon lamp is connected in series with the converter circuit. Start-up circuit may initiate the operation of the converter which creates a blinking phenomenon of LEDs and neon lamp. The controller intelligently indentifies the presence of the neon lamp and provides a sink current path for the neon lamp yet not to trigger the operation of the converter. Therefore, the controller provides a flicker-free feature in the applications where neon lamp is equipped with the wall switch**.**

Three-step analog dimming

The controller is designed with a proprietary three-step brightness control to adjust the LED brightness by using a wall switch. It simplifies the lighting applications without modifying any electrical wiring or the wall switch where applicable.

When AC power input is applied to the LED driver converter, the voltage at pin VDD rises to above a threshold of 16.5V to initiate the operation. The controller provides a first-level current sense reference VADJ at 1.0V while the converter provides the maximum brightness output.

When the AC power source input is removed, the VDD voltage maintains the bias of the IC operation before it decreases to its turn-off threshold of approximately 10.5V. If the AC source input is re-applied before the VDD drops below approximately 5.0V, OZ8027T maintains the brightness control function. It outputs a second brightness level dimming control by adjusting current sense reference VADJ to 400mV once the voltage at pin VDD exceed a threshold of approximately 16.5V.

Subsequently, if the AC power source input is removed and applied for the third time, OZ8027T outputs a third brightness level dimming control by adjusting current sense reference VADJ to 100mV. The operating frequency of third dimming level is reduced to 30kHz and achieve higher efficiency operation. Continuing the ON/OFF AC power source will repeat the brightness level settings described above.

LED Current Setting

Refer to the Typical Application Circuit, the LED current can be set as

$$I_{LED} = \frac{V_{ADJ}}{10 \times R_{CS}} \times \frac{N_p}{N_s} \times K$$

Where N_P is the number of turns of the primary winding; N_S is the number of turns of the secondary winding. R5 in Figure 6, connected at CS pin, is the current sense resistor R_{CS}. V_{ADJ} is reference voltage for internal OTA input; K is a coefficient parameter between 0.9 and 1, its value depends on the application circuit including transformer, power MOSFET parasitic capacitor etc.

Driver Output

A totem-pole drive output delivers the gate-drive signals to the external power MOSFET. The output is clamped at 17.4V to protect the external power MOSFET from being over stressed.

Operated at fix-frequency, discontinuous-current-mode in a Flyback converter, the controller provides an accurate output current over the variations of the input voltage. Also refer to Figure 3, the switch (power MOSFET) may not be turned on for the next cycle if the energy stored in the transformer T1 does not deplete to the output load (LEDs) within the cycle. When the feedback signal, FB drops below 0.4V, the controller is ready for the next-cycle turn-on of the switch. The pulse-skipping mode ensures Flyback converter operates at discontinuous-current-mode.

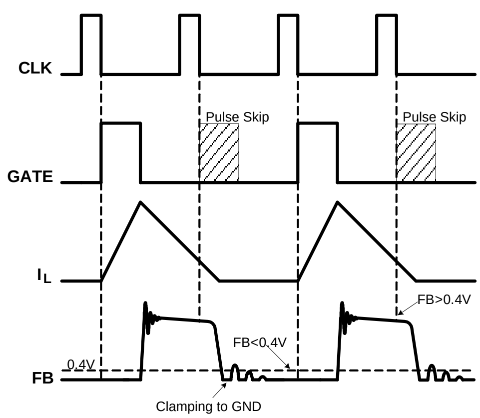


Figure 3

Line Regulation

The controller is designed to intelligently compensate the line voltage variations and tightly regulates the output. The feedback control relies on the coupling of the transformer with primary side winding sense alone can not provide accurate output when the AC input voltage varies from 85V to 265V. The power MOSFET turn-on time, turn-off time, the propagation delay in circuit and transformer coupling factor all affect the line regulation of the output. Design parameters are considered and lumped into the following formula to decide R7 resistor value properly.

$$R_7[kohm] \approx \frac{400 \times L_m[mH]}{R_{CS}} \times \frac{N_a}{N_p}$$

Where L_m is the magnetizing inductance of transformer, N_a is turn number of auxiliary winding. The average turn-off delay time for power MOSFET is estimated to be 50ns. Scale resistor R7 inverse proportionally when MOSFET has different characteristics. Properly select R7 to achieve accurate output when line voltage varies.

Leading-Edge Blanking of CS

When power MOSFET Q1 is turned on, a voltage spike may occur at CS pin due to parasitic in the application circuit. The controller is built-in with a filter at CS pin to ignore a 400ns leading-edge period at the turn-on of Q1. It is to avoid the MOSFET being turned off inadvertently. This feature eliminates an external RC filtering at CS pin.

Over current / short LED Protection

When a number of LEDs in a string are shorted, or the output terminal for the LEDs is shorted to ground, current flowing through the transformer rises sharply. When the current sense pin CS reaches 1.1V threshold, the controller turns off the output driver. It will not be turned on again until the next cycle starts. The cycle-by-cycle current-limit function prevents external components from being damaged under the fault conditions. In applications where the transformer design, such as leakage inductance, coupling coefficient may affect the sensed signal at CS pin. Since there is a 400ns blanking time at CS pin, the control may not be able to react fast if a sudden short to the LEDs creating the saturation to the transformer. A second protection level setting of CS pin at 1.6V is provided, when reached, will shut off the driver output. It will not be turned on until VDD drops below 10.5V followed by the rise to 16.5V threshold.

Output voltage drops under overload conditions. If either protection means above is not met while the feedback FB drops below 1V for longer than 14.4ms, the IC will shut off driver output. It will not be turned on until VDD voltage drops below 10.5V and then rises above 16.5V. In addition, the voltage of the auxiliary winding reflecting the voltage at the output, cannot sustain VDD bias voltage for the controller under the fault conditions. When VDD decreases below 10.5V, the internal start-up circuit operates to charge capacitor C7 at VDD pin to resume operation. The condition yields a hic-cup mode if the fault condition remains.

Open LED Protection

When the output load (LEDs) is opened, the control loop intends to regulate the rated current flowing through LEDs. The reflected voltage at the auxiliary winding increases. The FB pin as the divider of the reflected voltage at the auxiliary winding increases. If the FB voltage exceeds 3.6V during the turn-off period of the switch Q1, the controller will shut off the switching operation. The controller does not resume until VDD drops below 10.5V then rise to above 16.5V. The OVP protection threshold can therefore be designed by the following equation

$$V_{OUT\_OVP} = 3.6V \times \frac{N_s}{N_a} \times \frac{R_7 + R_8}{R_8}$$

In applications, when the power MOSFET is turned off, a ringing voltage spike will occur at FB pin due to parasitic capacitance of power MOSFET Q1 and leak inductor of transformer. This is illustrated in Figure 4

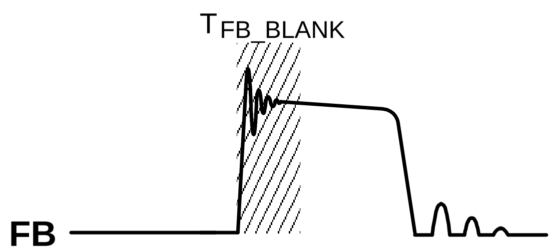


Figure 4: Ringing waveform of FB voltage

The controller provides a blanking period when Q1 is turned off to avoid a false-trigger at FB pin. The magnitude of the ringing waveform relates to the current flowing in the primary winding of the transformer. The controller provides the unique technique where blanking time for FB pin varies with the peak voltage of CS pin to achieve an optimal operation. Figure 5 illustrates the relationship between the peak voltage at CS pin and the blanking time at FB pin.

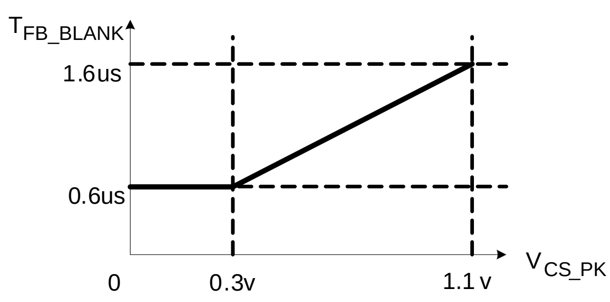


Figure 5: Dynamic Blanking time of FB

Over Voltage Protection

The reflected voltage at the auxiliary winding indicates the output voltage when Q1 is tuned off. The IC provides VDD over voltage protection function. When the VDD voltage exceeds 27.0V, the controller will turn off the output drive to the MOSFET Q1. To resume operation, the voltage at VDD needs to drop below 10.5V and then increase to the turn-on threshold of 16.5V.

Thermal Protection

Thermal protection occurs when the IC experiences a high junction temperature. The output drive is turned off once the junction temperature exceeds approximately 150ºC. It resumes normal operation when the junction temperature drops to or below approximately 120 ºC.

TYPICAL APPLICATION CIRCUIT

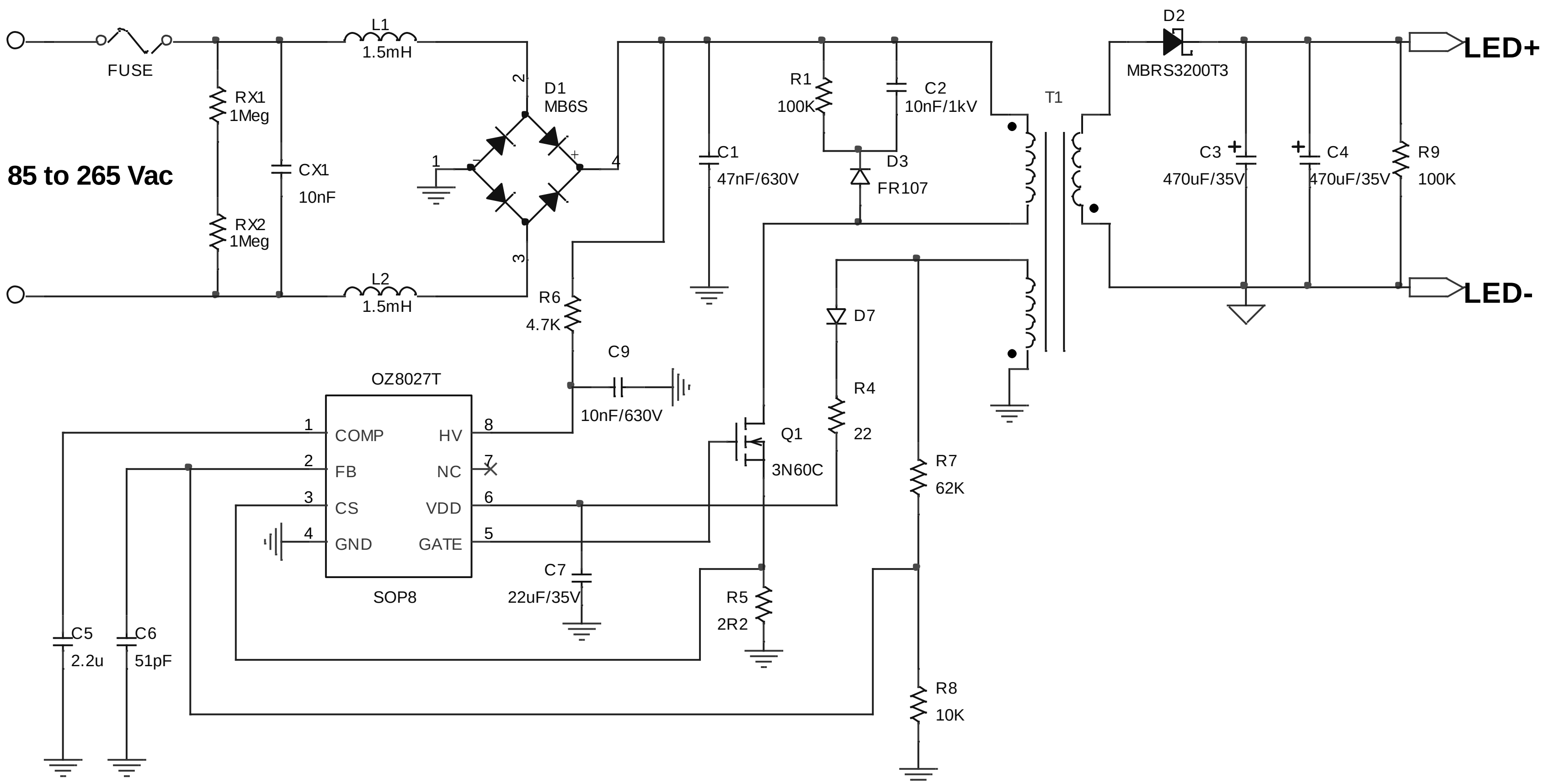
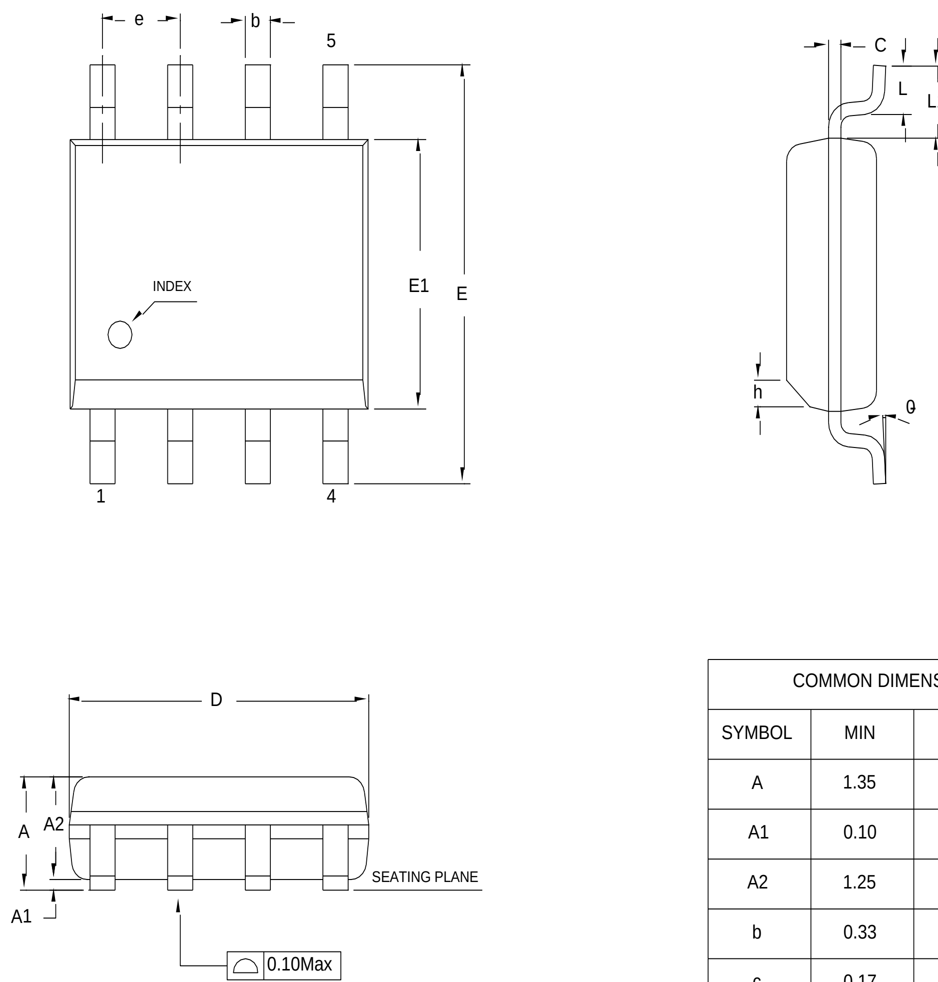


Figure 6: OZ8027T Typical Application Schematic

PACKAGE INFORMATION: 8L SOP, OZ8027T



NOTE:
1. REFER TO JEDEC STD MS-012 AA
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE

COMMON DIMENSIONS (MM)			
SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	-	-
b	0.33	-	0.51
c	0.17	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	-	1.27
L1	1.04 REF		
h	0.25	-	0.50
θ	0°	-	8°

IMPORTANT NOTICE